Robert W. Piatek

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Occupational Goal - Design and Development Engineering with emphasis on digital logic and microprocessor hardware - software design.

Education -

1973-1976 B.S.E.E. Electrical Engineering.
Rochester Institute of Technology, Rochester, New York

1971-1973 A.A.S. Electrical Technology.
Erie Community College, Buffalo, New York

Work Experience -

1998 - present *fishcamp engineering*, 105 W. Clark Ave., Orcutt CA 93455

President of design engineering services firm specializing in digital logic and embedded processor design. Details of previous projects are available at http://www.fishcamp.com.

- Developed a hardware reference platform for a major semiconductor company's wireless chipset. The system was DSP based to handle speech and signal processing algorithms required by the design. The system was demonstrated at the Comdex 2000 trade show.
- Responsible for the entire design of a low-light imaging camera for astro-photography and bio-sciences applications. The design entailed image sensor interface, FPGA based image processing logic, and software embedded in the camera itself as well as a host computer controlling application. Different versions of the camera have been marketed to the consumer amateur astronomy market as well as to OEMs in the life sciences field.
- Developed the image buffer subsystem for a professional astronomical observatory operated by NOAO. The design included 4GBytes of DDR2 memory controlled by an FPGA that performed data storage, formatting and low-level image processing functions on the image data. The system will be in use on various telescopes at Kit Peak in Tucson Arizona and Cerro Tololo, Chile.
- Developed an infrared imaging camera used to detect gas leaks at oil refineries. The system included an embedded processor running Linux and custom DSP algorithms implemented in a 4M gate FPGA. The FPGA logic design was written in VHDL code.
- Responsible for the digital base-band processor card for a 26Ghz LMDS terminal. The card included an embedded processor for station keeping and inter-terminal supervisory communications. All base-band signal processing was handled by four Xilinx FPGA devices. A DOCSIS compatible cable modem interface as well as analog I.F. interface circuitry to the rest of the radio's subsystems were also part of this project.

1993 - 1998 *ARK Telecom*, 2429 Professional Pkwy, Santa Maria, CA 93455
Director of hardware engineering in a telecommunications startup company specializing in frequency hopping TDMA Satcom products.

- Personally responsible for system architecture definition of the terminal as well as the logic implementation of the processor, burst controller and burst modem interface subsystems.
- Responsible for design and development of customer interfaces including voice, data, and E1 telephony circuit types.
- Worked with manufacturing personnel to develop automated test fixtures for all subassemblies released to production.

1980 - 1993 *COMTEL Corporation*, 2811 Airpark Drive, Santa Maria CA 93455
Manager of hardware engineering, TDMA Common Equipment Group.

- Managed a team of engineers in the design and development of hardware for a second generation 60 MBps and third generation 15MBps Time Division Multiple Access satellite communication terminal.
- Personally responsible for all aspects of the Burst Controller for several generations of Comtel's TDMA terminal product line. This subsystem consisted of a multi-processor architecture with a custom designed foreground processor and a general purpose NMOS background processor.
- Designed and developed a Soft-Decision VITERBI Forward Error Correction subsystem to be incorporated in COMTEL's 15 MBps TDMA Terminal.
- Responsible for the design, coding, and debug of the operator's interface console for the Comtel TDMA terminal line. This system was the operational hub of each node within a TDMA based satellite communication network and was responsible for executing commands and reporting status of the node to both a local operator as well as remotely to a network control center CPU. Program executed on a Hewlett-Packard desktop computer and consisted of over 14,000 lines of source code.
- Designed and developed hardware and software for a Monitor and Control system integrated into Comtel's TDMA product line. The system utilized a distributed processor architecture and provided both analog and digital input/output capability. The system was able to provide remote operation of unmanned earth stations from a network control center.

1976 - 1980 *Dow Jones and Company*, P.O. Box 300, Princeton, N.J. 08540
Senior Project Engineer

- Responsible for all of the data handling circuitry of a laser Flatbed facsimile system used to scan and transmit full-size pasteups of the *Wall Street Journal* pages. Circuitry consisted of the digitization logic and a scan line buffer memory used to interface with a serial satellite data circuit.
- Designed and developed a digital logic implementation of a data compression algorithm utilized by the flatbed facsimile system. This system allowed a 6:1 reduction in satellite channel bandwidth required for a typical page transmitted.
- Responsible for the design and implementation of a 'Smart' Control Panel for the flatbed facsimile system. This system used a distributed processor architecture and greatly simplified the installation, maintenance, and operator interface with the Flatbed system.

CO-OP Work Experience -

1973-1976 *XEROX Corporation*, Webster, New York.

- Assignments included testing and debug of digital systems. Completed projects in the area of mini-computer programming and interface. Worked six quarters full time, totaling 18 months over a three year period.

Security -

Have held D.O.D. (Secret) and D.O.E. (Q) security clearances.

Personal Data -

Date of Birth:	June 29, 1953	Health:	Excellent
		Height:	5'4"
Marital Status:	Married/Two children	Weight:	134